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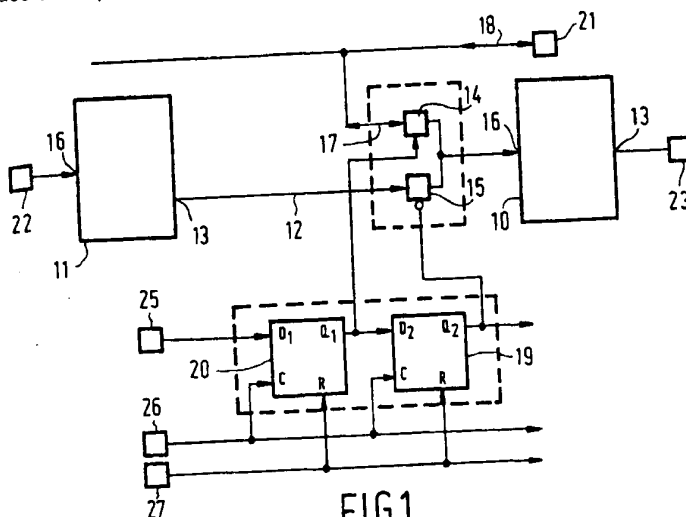
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NL-5656 AA Eindhoven(NL)**(54) **System for partitioning and testing submodule circuits of an integrated circuit.**

(57) A system for providing testing capability of individual submodules on an integrated circuit module. A test bus having a plurality of conductors is connected to selected internal ports of said submodules through three-way analog switches. Each three-way analog switch provides the capability to observe and

control an internal port through combination of the ON/OFF status of two transmission gates. Test patterns for controlling the transmission gates may be provided by onboard D flip-flops which are externally programmed to control or observe ports of an individual submodule.

**FIG.1****EP 0 434 137 A3**



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# EUROPEAN SEARCH REPORT

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EP 90 20 3300

DOCUMENTS CONSIDERED TO BE RELEVANT			Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
Category	Citation of document with indication, where appropriate, of relevant passages			
Y	EP-A-0 333 241 (PHILIPS' GLOEILAMPENF.) * abstract; figure 1 ** column 1, line 37 - column 2, line 39 ** column 6, lines 20 - 35 ** column 7, lines 28 - 38 ** column 9, lines 29 - 32 *	1,5,10,16	G 01 R 31/28 G 06 F 11/26	
Y	GB-A-2 085 171 (CONTROL DATA) * abstract; figure 1 ** page 1, lines 96 - 112 ** page 2, lines 51 - 52 ** page 3, lines 20 - 34 *	1,5,10,16		
A	IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS vol. 36, no. 2, May 1989, NEW YORK US pages 227 - 230; K.D.WAGNER et al.: "Design for Testability of Analog/Digital Networks" * page 229, left-hand column, lines 9 - 20; figures 2, 6-8 ** page 229, left-hand column, line 22 right-hand column, line 4 EP 90203300030* * page 230, left-hand column, lines 20 - 36 *	1,5,6,10, 16		
A	EDN ELECTRICAL DESIGN NEWS. vol. 33, no. 19, Septem- ber 1988, NEWTON, MASSACHUSETT pages 219 - 232; J.TURINO: "Circuit testability is critical for product success" * page 223, left-hand column, line 8 right-hand column, line 5 ** page 226, right-hand column, lines 4 - 8 *	1		
A,P	DE-C-3 839 289 (FRAUNHOFER-GES.) * abstract; figures 1, 2 ** column 4, lines 48 - 49 ** column 3, line 32 - column 4, line 45 *	1,5,10,16	TECHNICAL FIELDS SEARCHED (Int. Cl.5)  G 06 F G 01 R	
The present search report has been drawn up for all claims				
Place of search  Berlin		Date of completion of search  17 December 91	Examiner  FRITZ S C	
CATEGORY OF CITED DOCUMENTS X: particularly relevant if taken alone Y: particularly relevant if combined with another document of the same category A: technological background O: non-written disclosure P: intermediate document T: theory or principle underlying the invention			E: earlier patent document, but published on, or after the filing date D: document cited in the application L: document cited for other reasons  &: member of the same patent family, corresponding document	

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**EP 0 434 137 A2**

## SYSTEM FOR PARTITIONING AND TESTING SUBMODULE CIRCUITS OF AN INTEGRATED CIRCUIT.

The present invention relates to testing of integrated circuits by partitioning the integrated circuit into submodules by the use of three-way analog switches, and individually testing the partitioned submodules. Specifically, a technique which reduces the number of required transmission gates, while increasing the level of testability is described.

5 The design of integrated circuits generally consists of multiple subcircuits, referred to hereinafter as submodules, which are interconnected to form an overall module circuit. After fabrication, each module circuit is tested prior to shipment in a variety of ways to establish that it is operating properly.

The module may be tested as a single entity by placing known electrical signals on the module circuit input ports while observing output phenomena on the output ports. The disadvantage in testing the module  
10 device from external input and output ports results because the number of test cases required grows exponentially with the complexity of the module. Signal masking effects make it difficult to exercise all submodules, and the settling time varies greatly between submodules. This is especially significant for analog circuits.

Various techniques have been proposed to employ a "divide and conquer" strategy by partitioning the  
15 module into submodules in order that each submodule may be effectively isolated from the other submodules, and tested in its isolated condition to determine that each submodule works correctly.

Circuit techniques are employed on the individual module for gaining access to the internal ports of each submodule which has no direct connection to any external I/O pad of the module.

These techniques have been employed for digital and analog circuit modules, as well as for modules  
20 which are mixed analog digital circuits. One such technique, is described in an article entitled "Design for Testability for Mixed Analog/Digital ASICs" IEEE, 1988, Custom Integrated Circuits Conference, pages 16.5.1-16.5.4. This technique divides a mixed analog/digital ASIC chip into analog blocks and digital blocks, and uses multiplexers connected to internal ports between the blocks, permitting that internal port to be either controlled or observed from external I/O pads, depending on test mode control signals applied to the  
25 multiplexers.

In a paper entitled "Design for Testability of Mixed Signal Integrated Circuits" by Kenneth Wagner and T.W. Williams, 1988 International Test Conference, paper 39.1 pages 823-828, there is described a technique for providing macrotests on an integrated circuit. The circuit module is partitioned into a number of submodules, or macros, which define their own specific function.

30 In carrying out the partitioning of the circuit module, analog macro inputs are isolated and controlled so that macro outputs may be observed, via the use of analog multiplexers. The use of multiplexers requires an undesirable amount of module layout area overhead, as well as the necessity of running numerous additional wires from the multiplexer to various internal ports. There is also a limitation on the number of test configurations which may be conducted.

35

#### Summary of the Invention

It is an object of the present invention to provide a system for partitioning a circuit module into individual testable submodules.

40 It is a more specific object of this invention to partition a circuit module using a minimum number of switching elements to preserve layout area.

It is yet another object of this invention to provide for a system for dynamically partitioning submodules within a circuit module in accordance with the sequence of data input to the device.

These and other objects of the invention are provided by a circuit for testing analog submodules,  
45 arranged in an inter-connected network including a succeeding submodule which receives an input from a preceding submodule, on an integrated circuit, the circuit comprising:

- a) a test bus comprising a plurality of conductors disposed on said integrated circuit, one of said conductors terminating in an input/output connection;
- b) at least one three-way analog switch, each switch comprising an output connection connected to an  
50 input of the succeeding submodule, an input/output connection connected to said one conductor, and an input connection connected to an output of the preceding submodule; and
- c) means for configuring the at least one switch to assume one of the following states:
  - i) a first state in which the input of the succeeding submodule is connected to the output of the preceding submodule, and not to the test bus;
  - ii) a second state in which the input of the succeeding submodule is connected to the test bus and

not to the preceding submodule; and

iii) a third state in which the output of the preceding submodule is connected to both the input of the succeeding submodule and the test bus.

Extra circuitry is added to the circuit module which will partition the module into individual submodules.

5 In a first embodiment of the invention, the circuit is characterized in that each switch further comprises first and second transmission gates connected together at one end. Thus carrying out the invention, analog switches consisting of transmission gates are used to access the normal signal paths between submodules. The transmission gates are advantageously located near an internal input port of a submodule in the path of a signal line connecting the internal port to another internal output port of a second submodule. The  
10 transmission gates are additionally connected to a conductor of a test bus.

Each of the submodules having ports which are to be asserted or observed are connected through a transmission gate to the adjacent submodule. A logic circuit is provided for setting the switch state so that identified internal ports are either connected to a test bus conductor, which will supply an asserted condition to the input port, or the conductor is connected to the input port without disturbing the normal paths through  
15 the module, permitting observation of the signal conditions on the input port.

Extra input/output paths may be added to the module circuit substrate to accommodate shifting in data to the logic circuit, as well as provide direct access to one of the test bus conductors.

#### Brief Description of the Figures

20 Figure 1 illustrates the system for testing, implemented between two submodules 10 and 11, in accordance with a preferred embodiment. The analog switch is implemented using two transmission gates 14 and 15.

Figure 2 illustrates a three-transmission gate implementation of the analog switch, having additional test  
25 capability over the embodiment of Figure 1.

Figure 3 shows an embodiment of the invention for providing an observability only function between two circuit submodules.

Figure 4 illustrates an embodiment providing controllability only of an internal port of a submodule.

Figure 5 illustrates a specific embodiment of the invention to partition a circuit module into two  
30 submodules.

Figure 6 illustrates a specific embodiment of the invention for implementing a test scheme on a fluorescent light ballast integrated circuit.

#### Description of the Preferred Embodiment

35 Figure 1 illustrates in general terms how two submodules 10 and 11 may be partitioned from a circuit module in accordance with a test system of the preferred embodiment. The submodules 10 and 11 may be analog circuit blocks which exist on an integrated circuit as a single circuit. Partitioning the integrated circuit into submodules 10 and 11 permits the blocks to be tested in individual sections. The submodules 10 and  
40 11 generally have an input port 16 and an output port 13. Usually such submodules would have more than one input, as well as more than one output.

The partitioning is accomplished with an analog switch 17 which is disposed adjacent an input port 16 of a module 10. The analog switch 17 is controlled from a pair of D flip-flops 19 and 20.

45 The analog switch 17 comprises two transmission gates 14 and 15. In CMOS fabrication processes, these transmission gates may be implemented by parallelly connected N-channel and P-channel transistors having gate connections connected through an inverter. These known transmission gates may be operated so that 14 is closed, and 15 is open, thus isolating output port 13 from input port 16, while connecting input port 16 to the bus conductor 18. A test signal can then be asserted to input port 16 via test pad 21.

50 By keeping both transmission gates 14 and 15 closed, a signal from output port 13 may be routed to a test bus conductor 18. In the normal operation state, the input port 16 and output port 13 are connected together. This is done by keeping 15 closed and 14 open.

Thus, it can be seen that the analog switch 17 permits both observability of input port 16 as well as the ability to assert a control signal on input port 16.

55 The configuration shown will permit verifying the integrity of the normal signal path 12. In so doing, the output signal from submodule 11 may be observed at test pad 21, or a desired input signal may be asserted on test pad 21, and the output port 13 of submodule 10 may be observed through a pad 23.

Control over the analog switch 17 is provided by D flip-flops 19 and 20. The D flip-flops 19 and 20 provide on their Q outputs an enable signal to transmission gate 14 and transmission gate 15. Thus, by

programming the flip-flops 19 and 20, it is possible to establish controllability over port 16 or observability over port 13.

The data for establishing a test condition is applied to a pad 28 on the integrated circuit. A clock pulse is supplied to a pad 26, clocking in serial data applied to the input pad 28. Thus, by clocking in two bits of input data, the transmission gates 14 and 15 may be set in accordance with the following Table.

TABLE I

Mode	Transmission Gates		Function
	14	15	
1	OFF	ON	Normal operation: output 13 of module 11 goes to input 16 of module 10 via 15
2	ON	OFF	Control input of module 10: external test signal goes to input 16 via 14
3	ON	ON	Observe output of module 11: output 13 goes to test pad via 15 and 14
4	OFF	OFF	Isolation: both output 13 and input 16 are isolated

It should be noted that mode 3 in Table 1 demonstrates that when the output 13 is observed, this output is observed with the usual loading presented at input terminal 16. The total load experienced by output 16 is the parallel combination of the normal load at port 16, and the extra load due to test pad 21 and external measuring instruments. However, for the most part, this mode permits accurate monitoring of the signal from output port 13 of submodule 11 under normal conditions.

The foregoing embodiment using two transmission gates provides a reasonable compromise between conserving layout area on the integrated circuit surface and testability. It is possible to employ a third transmission gate 24 as shown in Figure 2. The third transmission gate 24 will permit isolating the output node 13 during an observe function from the input port 16. The third transmission gate 24 can shunt the normal output signal directly to the test bus conductor 18, while transmission gates 14 and 15 are open, effectively isolating input port 16 from output port 13. However, it is considered that the foregoing two transmission gate embodiment is preferred to conserve on layout space for the integrated circuit substrate in the face of only marginal increases in testability when transmission gate 24 is employed.

Other adaptations of the embodiment shown in Figure 1 can be seen in Figures 3 and 4. In the case of Figure 3, this simplified version of the testing scheme in accordance with the invention permit observing the condition on output port 13 under actual operating conditions. In the case of Figure 4, the input port 16 may be asserted with a control signal from external test pad 18 while output port 13 is isolated.

It must be emphasized that the embodiments of Figures 1, 2 and 3 permit testing of the normal signal path 12 for each submodule. Therefore, once each individual submodule has been verified as testing successfully, the continuity of the interconnections between submodules is insured.

The sequence for testing the submodules 10 and 11 can be shown in Table II below, demonstrating the state of flip-flops 19 and 20 can be set by shifting in data sequentially to carry out the five functions noted. The two flip-flops 19 and 20 comprise a two-bit shift register which may be readily programmed through the data input 28 to implement the four described functions. A clock pulse 26, associated with shift registers, is applied to shift in each of the serial data bits.

TABLE II

Action	Flip-Flops		Transm. Gates		Function
	20	19	14	15	
RESET	0	0	OFF	ON	Normal operation
Shift-in 1	1	0	ON	ON	Observe output of module 11
Shift-in 1	1	1	ON	OFF	Control input of module 10
Shift-in 0	0	1	OFF	OFF	Isolation
Shift-in 0	0	0	OFF	ON	Back to normal operation

A reset pad 27 is shown connected to reset inputs of the flip-flops 19 and 20. The reset permits restoring a circuit to its normal functioning condition, wherein transmission gates 14 and 15 are rendered in the unswitched state, with transmission gate 15 being conductive and transmission gate 14 being non-conductive.

The foregoing principles of partitioning circuits within an integrated circuit into submodules using three-way analog switches are shown implemented in Figure 5 in a more realistic configuration of an integrated circuit.

Figure 5 illustrates the probable connections from a subsequent submodule 10 to a preceding submodule 11. A second output port 13a is located in the succeeding submodule 10, and is connected through three-way analog switch 30 to the preceding submodule 11. Analog switch 30 has an input connected to the test bus conductor 31. The second bus conductor 31 may be employed to assert a signal condition on input 16a, or for routing the output 13a of submodule 10 to the bus conductor 31, depending on the state of analog switch 30. The switching states for the analog switch 30 is controlled by a pair of D flip-flops 32 serially connected with the aforesaid described D flip-flops 19 and 20 which control analog switch 17.

There is also shown analog multiplexers 37 and 39, which also consist of two transmission gates each. These analog multiplexers permit the reduction in the number of circuit pads needed for the integrated circuit. The analog multiplexer 37 permits the input pad 22, depending on the states of D flip-flop 33, to be connected either to the test bus 18 or an input 16 of submodule 11. Thus, the required input and output pads are kept to a minimum, consistent with good integrated circuit design. An in/out pad 21 is shown which may also be connected through an analog multiplexer 38. This permits the input/output pad 21 to access either test bus conductor 31, or a port of another submodule, which is not shown in this Figure. A D flip-flop 35 is used to control the switching state of analog multiplexer 38.

More than one test bus conductor can be accessed from a test pad by using larger multiplexers. For example, a 4 to 1 multiplexer can access either one of three bus conductors, or a port of some submodule. In this case, two flip-flops are necessary to control the switching state of the multiplexer.

By mapping more of the test functions to a single input/output pin, it is possible to hold the extra pad requirements to a minimum. However, it should be noted that only one internal output port at a time may be observed when using such multiplexing techniques. Thus, it may be necessary to assign more than one test mode for a given submodule.

Using the foregoing test scheme, area overhead on the substrate arises from analog switches, multiplexers, and any additional I/O pads located on the substrate. There is extra channel area required for routing the test bus and the control lines for the flip-flop. However, for many applications, these sources of area overhead are advantageous over other techniques for analog testing.

In applying the foregoing principles, it is clear that the number of conductors N in the test bus is proportional to the sum of the number of internal input ports which must be controlled simultaneously for a given submodule, and the number of internal output ports M which must be simultaneously observed for the testing of a submodule.

Finally, a specific implementation of the principles of the invention are shown in Figure 6 for an integrated circuit serving as a ballast chip in a fluorescent lighting system. This common integrated circuit is

exemplary only of how integrated circuits in general may be partitioned to permit submodule testing.

In this particular design, the ballast chip consists of four submodules. These include the driver module 69, control module 66, power supply module 63 and protection module 65. In establishing partitioning use is made of the fact that this integrated circuit already includes subdivisions into the four submodules. The three-way analog switches will be located to control selected internal ports of each of the four submodules. In establishing internal ports which will be controlled or observed, the following summary of Table III can be made:

TABLE III

Module.Port	From	Type	Function
CONTRL.PWMOFF	PRTCTN.PWMOFF	Logic	PWM on/off
CONTRL.PPOFF	PRTCTN.PPOFF	Logic	Push-Pull circuit on/off
CONTRL.FSWP	PRTCTN.FSWP	Analog	Sweeps oscillation freq.
PRTCTN.VBE1	SUPPLY.VBE1	Analog	Decreases w/temperature
PRTCTN.WIDTH	CONTRL.WIDTH	Logic	Anti-capacitive load

Given the number of internal ports to be controlled or observed, the total number of conductors in the test bus is found through the following Table:

TABLE IV

Testing Module	Control Input	Observe Output	# Wire
CONTRL	{PWMOFF, PPOFF, FSWP}	{WIDTH}	4
PRTCTN	{VBE1, WIDTH}	{PWMOFF, PPOFF, FSWP}	5
	Alternatively, we can observe outputs one at a time: {VBE1, WIDTH} {VBE1, WIDTH} {VBE1, WIDTH}	{PWMOFF} {PPOFF} {FSWP}	3
SUPPLY		{VBE1}	1

This Table will establish for each module which inputs are to be asserted simultaneously and which output ports are to be observed. The number of required bus conductors for each of the tests of Table IV can be reduced if ports are observed sequentially. Thus, when testing protection module PRTCTN, by observing only one of PWMOFF, PPOFF, FSWP at a time, the number of conductors may be reduced to three, two for asserting control signals on VBE1, WIDTH and one for observing at different times PWMOFF, PPOFF and FSWP. This increases testing time for submodule PRTCTN since ports are being sequentially



observed.

The number of conductors adds chip area overhead to the module. This consideration must be balanced with the need for conserving testing time. Table V illustrates one solution which is considered a good compromise between the number of bus conductors and testing time.

As Table V indicates, wires 46, 47 and 48 are connected to control FSWP, PWMOFF, PPOFF, while wire 45 observes the width during mode number 1. The remaining entries of the Table show three additional test modes, wherein the four wires of the bus are used to implement the indicated "C" control signals on the control ports, while simultaneously observing the indicated "O" signals on the observe ports.

Having now decided which conductors of the bus are to be routed to a given port during a test, using the analog switches of Figure 6, it is possible to map each of the ports set forth in Table V to either an output multiplexer 49 for observing signals, or an input multiplexer 43 for asserting the control signals for each of the tests set forth in Table V.

TABLE V

Mode	Testing	Wire #45	Wire #46	Wire #47	Wire #48
1	CONTRL	WIDTH (o)	FSWP (c)	PWMOFF (c)	PPOFF (c)
2	PRTCTN	WIDTH (c)	VBE1 (c)	PWMOFF (o)	PPOFF (o)
3	PRTCTN	WIDTH (c)	VBE1 (c)	FSWP (o)	
4	SUPPLY		VBE1 (o)		

A multiplexer 43 is shown which multiplexes normal input signals OC (corresponding to an over-current sensed condition), OV (corresponding to an over-voltage condition), and VLAMP (corresponding to the voltage across the fluorescent lamp). These pins may additionally be used during tests of the integrated circuit to apply any three required control signals to any three test bus conductors 45, 46 and 47.

The test bus conductors 45, 46, 47 and 48 are connected to respective transmission gates 61 and 62, 57, 58 and 59 for either observing or asserting a control condition on an internal port of the submodules. As can be seen, analog switches 57, 58 and 59 can assert the required control signal input from circuit pads 40, 41 and 42 on each of the inputs FSWP, PWMOFF, PPOFF of the control submodule 66.

This assert condition is established by the states of flip-flops 75 and 73, such as to make sure the switches assume a state for asserting these conditions.

The multiplexer 49 will permit observing an internal port condition on any of test buses 46, 47 and 48. The multiplexer 49 will, under control of flip-flop 72, connect circuit pad 50 with bus conductor 46, circuit pad 51 with bus conductor 47, and circuit pad 52 with bus conductor pad 48. An analog multiplexer 55 will permit circuit pad 53 to be connected to conductor 45. A circuit pad 54 will permit observation of bus 45 under control of flip-flop 71.

As will be obvious, the circuit pads 40, 41 and 42 and 50, 51, 52, 53 and 54 are normal signal input and output connections for the integrated circuit of Figure 6. The use of the multiplexers 43, 49, 55 and 56 will therefore maintain the circuit pinout at a minimum.

Additional analog switches 61 and 62 are connected to isolate the PRTCTN 65 from the CONTRL 66 submodule and from the supply 63 submodule. These gates are enabled by D flip-flop circuit 74. It will be obvious that flip-flop circuit 74 provides a four-bit output and flip-flop circuit 73 provides a three-bit output for controlling the respective analog switches. As will be evident from Table V, by appropriately setting each of the flip-flop circuits 73 and 74, the internal ports WIDTH and VBE1 can either be controlled or observed via the test bus conductors 45 and 46.

As was described with the earlier Figures, three additional pads are employed for clocking in test pattern data to the flip-flops 71 through 75. This includes data input pad 28, a clock pad 26 and a mode pad 27 for resetting the flip-flops. In the reset condition, the integrated circuit is set for its normal operation.

Thus, there is described with respect to several examples, implementation of a test scheme for integrated circuits. The test scheme is useful for testing to provide isolation of defects within the integrated circuit. This is useful in that integrated circuits may tend to have the same submodule defective. By early location of a particular defective submodule, corrections to the manufacturing process may be implemented at an early stage. Additionally, potential savings in testing time are recognized. This occurs as in analog circuits in particular, a settling time is necessary for each part of the entire circuit. By partitioning the circuit,

variable time steps for testing of different portions may be utilized, rather than waiting a test time equal to that for the module having the longest required settling time.

The system permits different tests to be executed during different portions of the manufacturing process. For instance, it is common to do a wafer probe test, followed by a package test in integrated circuit manufacture. It is possible to set up distinctly different tests using the foregoing programmable feature of the D flip-flops.

Thus there is described an invention, including to several examples, which will be more particularly disclosed, but not limited by, the claims which follow.

## 10 Claims

1. A circuit for testing analog submodules, arranged in an interconnected network including a succeeding submodule which receives an input from a preceding submodule, on an integrated circuit, the circuit comprising:
  - a) a test bus comprising a plurality of conductors disposed on said integrated circuit, one of said conductors terminating in an input/output connection;
  - b) at least one three-way analog switch, each switch comprising an output connection connected to an input of the succeeding submodule, an input/output connection connected to said one conductor, and an input connection connected to an output of the preceding submodule; and
  - c) means for configuring the at least one switch to assume one of the following states:
    - i) a first state in which the input of the succeeding submodule is connected to the output of the preceding submodule, and not to the test bus;
    - ii) a second state in which the input of the succeeding submodule is connected to the test bus and not to the preceding submodule; and
    - iii) a third state in which the output of the preceding submodule is connected to both the input of the succeeding submodule and the test bus.
2. The circuit of claim 1 characterized in that each switch further comprises first and second transmission gates connected together at one end.
3. The circuit of claim 2 characterized in that the means for configuring the at least one switch comprise a plurality of flip-flops, each associated with at least one of said transmission gates, said flip-flops being arranged in series to receive on a data-in conductor a bit data pattern, the first and second transmission gates within a single switch being associated with separate ones of the flip-flops.
4. The circuit of claim 3 wherein said flip-flops are D-type flip-flops, further including a clock input connected together.
5. A circuit for testing electronic submodules on a common substrate, at least one of said submodules having an input for receiving an output signal of a preceding submodule comprising:
  - a test bus comprising a plurality of conductors connected at one end to a plurality of test pads on said substrate;
  - an intermediate analog switch located adjacent each input of a submodule having an output terminal connected to said submodule input, and an input terminal connected to an output of a preceding submodule, and an input/output terminal connected to one of said plurality of conductors;
  - an input analog multiplexer having an input connected to a signal input pad of said common substrate, a first output to one of said test bus conductors, and a second output connected to an input of said preceding submodule, selectively permitting a signal to be supplied from said signal input to said preceding submodule and said one test bus conductor;
  - an output analog multiplexer having a first input connected to an output of said succeeding submodule, a second input terminal connected to said one test bus conductor, and an output terminal connected to a signal output pad; and,
  - a plurality of flip-flops, each flip-flop being located adjacent each of said analog switches and

multiplexers and connected to operate each analog switch and multiplexer to effectively isolate each submodule, and provide a signal to individual isolated submodules, and provide an output signal from said isolated submodules to said test pad.

- 5 6. A circuit for testing electronic submodules according to claim 5 further comprising:

10 a second intermediate analog switch located at a second input of said preceding module, having an input connected to a second output connection of said succeeding module, an input/output connection connected to a second conductor of said test bus, and an output connection connected to said preceding module second input, said analog switch being connected to one of said flip-flops for isolating said preceding module second input from said succeeding module; and,

an input/output test pad connected to said second conductor for receiving or supplying a signal to said input/output connection of said second intermediate analog switch.

- 15 7. The circuit of claim 5 further comprising a data input pad on said substrate, connected to supply data to each of said flip-flops.

20 8. The circuit of claim 6 further comprising a reset pad on said substrate connected to reset said flip-flops, said reset flip-flops establishing input/output connections of said modules to a normal configuration.

- 25 9. The circuit of claim 7 wherein said flip-flops are serially connected, and a test data configuration is shifted into said flip-flops through said data input pad.

30 10. In an integrated circuit having a plurality of circuit elements comprising a plurality of submodules, one of said submodules including an output connected to an input of an adjacent module, and an input connected to an output of said adjacent module, a circuit for testing said submodules individually comprising:

first and second analog switches located adjacent respective of said inputs having a first connection connected to said inputs, a second connection connected to outputs of an adjacent submodule, and third connections;

35 a test bus on said integrated substrate having a first conductor connected to said first analog switch third connection, and a second conductor connected to said second analog switch third connection; and,

40 first and second digital flip-flop circuits located adjacent respective of said first and second analog switches, said digital flip-flops having a data input for receiving test data which identifies a test state for said analog switches, whereby input and output connections of one of said modules are connected to said first and second conductors.

- 45 11. The circuit for testing of claim 10 further comprising:

an analog multiplexer connecting an input pad of said integrated circuit to said first test bus conductor, and a second input of said one submodule; and,

50 a third flip-flop connected to said analog multiplexer for permitting a signal to be selectively routed through said input pad to said one submodule second input, or said test bus first conductor.

12. The circuit of claim 11 further comprising:

55 a second analog multiplexer connected to said test bus first conductor, and to a second output of said adjacent module, and having an output terminal connected to an output pad on said substrate; and,

a fourth flip-flop connected to switch said second analog multiplexer in response to test data supplied to said fourth flip-flop, whereby an output signal from said one submodule may be applied through said

first analog switch and second analog multiplexer to said output pad.

13. The circuit of claim 12 further comprising:

5 a third analog multiplexer connected to said test bus second conductor, and to an input/output pad; and,

a fifth flip-flop connected to enable said third analog multiplexer in response to said test data.

10 14. The circuit of claim 10 wherein said digital flip-flops are D-type flip-flops having data inputs serially connected together with a data input pad on said integrated circuit, said flip-flops having a clock connection connected to a test clock pad on said substrate, permitting test data to be serially supplied to said flip-flops to identify a submodule to be tested.

15 15. The circuit of claim 14 further comprising a mode control pad on said substrate connected to a reset input of said flip-flops which permit said test data to be cleared from said flip-flops.

16. A system located on a circuit module for providing a testing capability of individual submodules of said circuit module, said individual submodules being interconnected through a plurality of output and input  
20 ports on each submodule comprising:

a test bus having a plurality of conductors equal in number to the sum of the number of ports on a submodule to be controlled during a test, and the number of ports to be observed at the same time;

25 a first multiplexer connected to said plurality of conductors for selectively asserting control signals on a first group of said conductors equal to said number of ports to be controlled;

a second multiplexer connected to said plurality of conductors for selectively observing signals on a second group of said conductors equal to the number of ports to be observed;

30 analog switch means for mapping said ports to be controlled to said first group of conductors, and mapping said ports to be observed to said second group of conductors; and,

35 digital logic control means connected to said first and second multiplexers and said analog switch means for connecting and enabling said ports to be asserted and observed when a test pattern is loaded in said logic means.

17. A system for providing a testing capability according to claim 16 wherein said analog switch means interrupt normal submodule interconnections when enabled by said digital logic control means, and  
40 restore normal submodule interconnections when disabled by said digital logic means.

18. The system of claim 17 wherein said first multiplexer has input connections which supply signals to be asserted on said number of ports to be controlled when enabled, and which receive normal module input signals when disabled by said digital logic means, supplying said normal module input signals to  
45 input ports of said submodules for normal circuit operation.

19. The system of claim 17 wherein said second multiplexer is connected to output ports of said submodules for providing normal module operating signals from said ports when disabled by said digital logic means.

50 20. The system of claim 16 wherein said digital logic means comprise a plurality of D flip-flops serially connected to each other, each D flip-flop being located adjacent a respective analog multiplexer or analog switch means, and connected to control said adjacent multiplexer or analog switch means.

55 21. The system of claim 20 wherein said serially connected D flip-flops are connected to receive serial data defining a test pattern in response to a clock signal.

22. The system of claim 21 wherein said D flip-flops have a reset input which restores said analog

multiplexer and analog switch means to a disabled condition, permitting normal circuit operation.

23. The circuit of claim 3, further comprising a plurality of three-way analog switches, the input connection of the first transmission gate in each switch being coupled with a first one of the flip-flops, the input connection of the second transmission gate in each switch being coupled with a second one of the flip-flops.
24. The circuit of claim 3 wherein
  - a) the first transmission gate has:
    - i) an input coupled with a first one of the flip-flops;
    - ii) an input/output connection coupled with the test bus; and
    - iii) an output coupled with the succeeding submodule; and
  - b) the second transmission gate has:
    - i) a first input coupled with the preceding submodule;
    - ii) a second input coupled with a second one of the flip-flops; and
    - iii) an output coupled with the output of the first transmission gate.
25. The circuit of claim 3 wherein the three-way analog switch further comprises a third transmission gate coupled between the input connection of the three-way analog switch and the input/output connection of the three-way analog switch.
26. The circuit of claim 3 further comprising a data input connection connected to supply data to said flip-flops, and wherein the first and second flip-flops are serially connected, and a test data configuration is shifted into said flip-flops through said data input connection.
27. The circuit of claim 3 further comprising a reset connection connected to reset said flip-flops, said reset establishing input/output connections of said modules to a normal configuration.

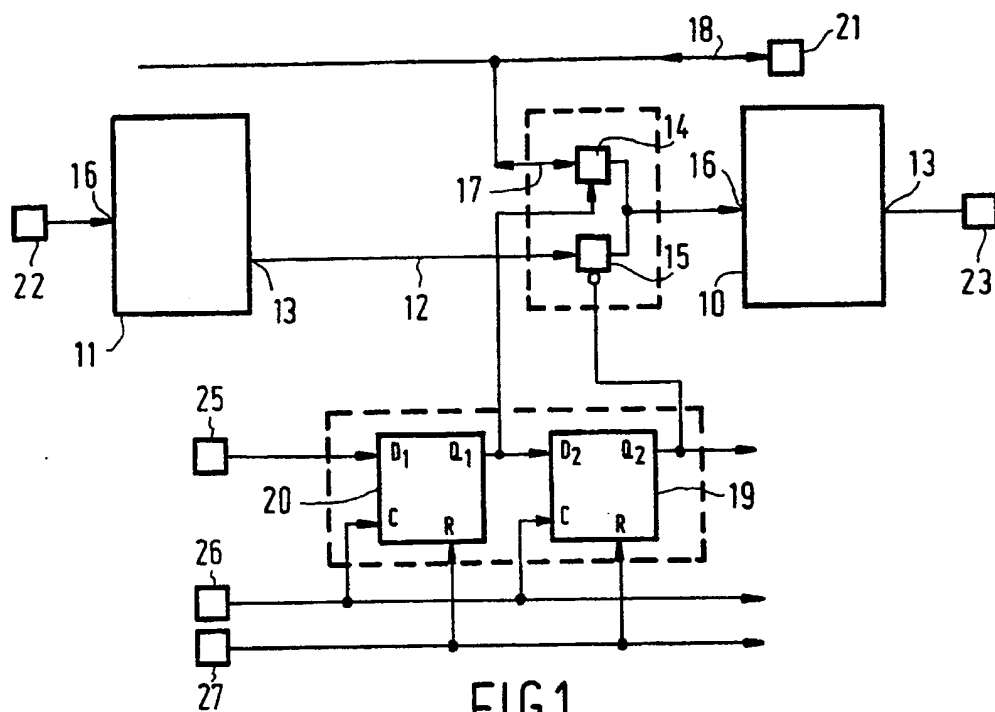


FIG.1

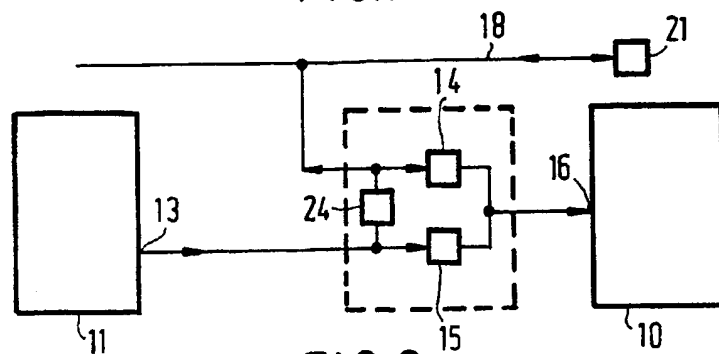


FIG.2

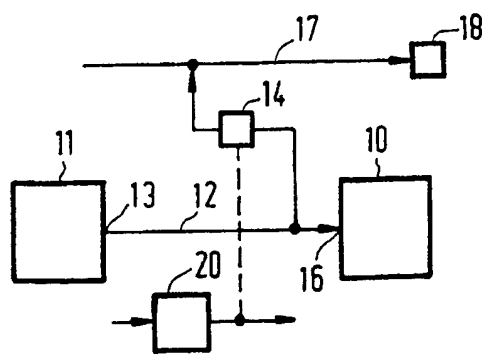


FIG.3

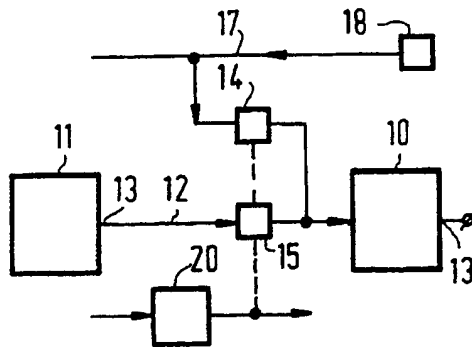


FIG.4

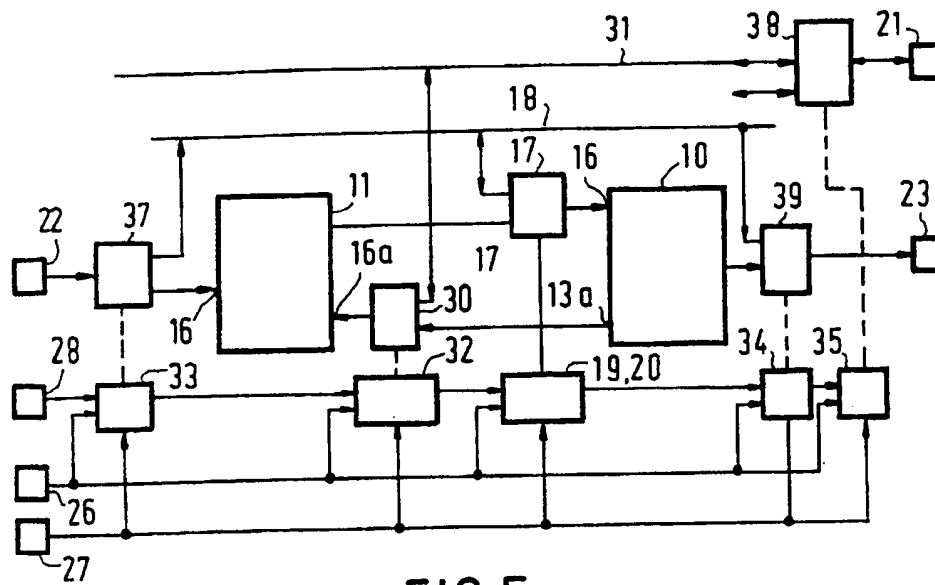


FIG. 5

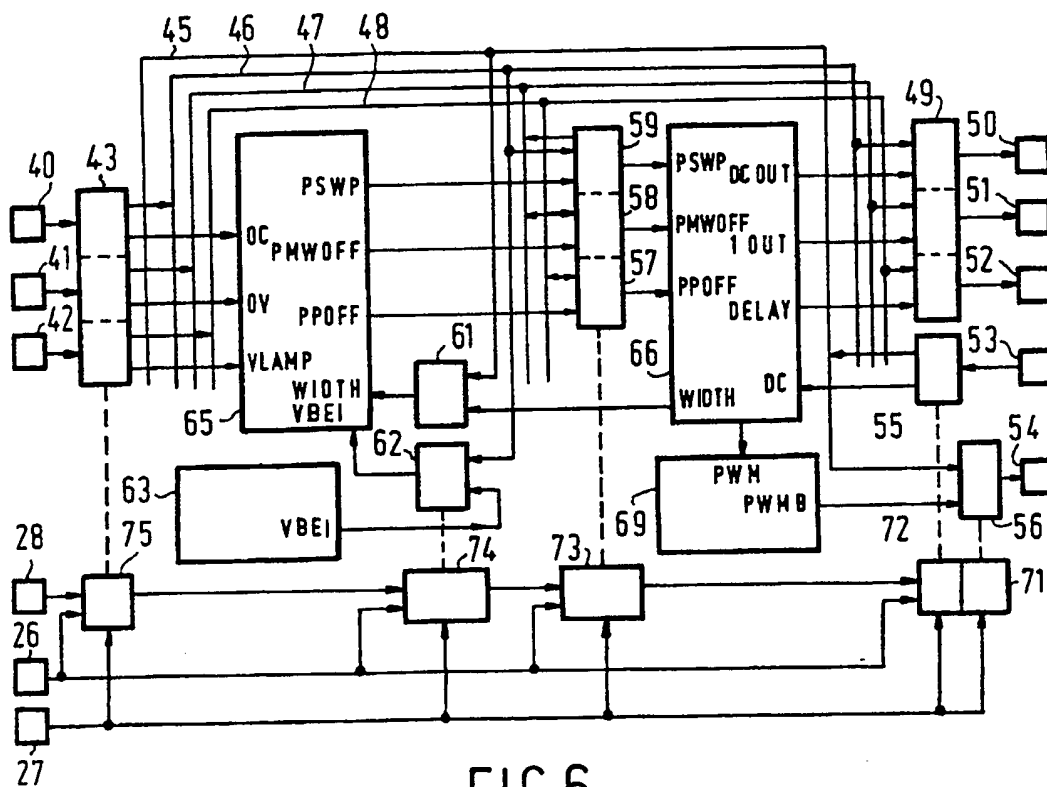


FIG.6